Remarks

The referenced patent application has been reviewed in light of the referenced Final Office Action and Advisory Action.

In the Claims, claims 1-28 are pending in the referenced application. Claims 1, 5-10, 15 and 20 are amended in this Response.

I. Claim Rejections -35 USC § 102(b)

The Office Action has rejected 1-5 and 10-24 under 35 U.S.C. § 102(b) as being as being anticipated by Zalewski et al., US Patent No. 6260068 B1 (Zalewski). However, the Office Action has failed to meet its burden of makings a prima facie case of anticipation for the claims, and such rejections should be withdrawn.

"[F]or anticipation under 35 U.S.C. 102, the reference must teach *every aspect* of the claimed invention ..." MPEP 706.02 (emphasis added). "The identical invention must be shown *in as complete detail as contained in the ... claim*." *Richardson v., Suzuki Motor Co.*, 868 F. 2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989) (emphasis added). Zalewski simply fails to disclose every aspect of the inventions claimed in Claims 1-5 and 10-24. The Examiner has therefore failed to meet his burden of making a prima facie case of anticipation.

Zalewski pertains to an "inventive software architecture" (Zalewski, Col. 5, line 56) that allows software (operating systems) to migrate resources from one partition to another. (Zalewski, Abstract). The "inventive system operation" of Zalewski may be performed by "any operating system" that implements the "software system requirements" disclosed in the Specification. (Zalewski, Col. 5, lines 59-61). Thus, Zalewski is directed to a manner for

allowing software operating systems to cooperate to migrate resources from one partition to another. (Zalewski, Abstract, emphasis added).

The push model disclosed in Zalewksi is different from the scheme claimed by Applicants. Fig. 9 of Zalwesky makes clear that what is disclosed by Zalewski requires that a second OS instance requests a resource from a first OS instance. "In accordance with the push model used in the present invention, operating system instance 1 (1008) must agree to the transfer of the requested resource 1010 to operating system instance 2 (1018). If operating system instance 1 (1008) agrees, it quiesces the resource 1010 as indicated in step 904." (Zalewsky, Col. 30, lines 1-6). Thus, Zalewsky is directed toward allowing OS instances to cooperate in order to provide additional resources for an instance that needs them. A resource is not quiesced until the resource has been requested by another instance.

In contrast, Applicants claim a different scheme that is, in some ways, the complete opposite of the scheme disclosed by Zalewski. Rather than re-allocating a resource based on whether a second instance *does need* it, Applicants' claims focus on de-allocating a resource if a first logical processor *doesn't need* it (due to being idle). The de-allocated resource becomes available to other logical processors when the logical processor has no further tasks for scheduling. This distinction is just one of many patentable distinctions between what is disclosed in Zalewsky and what is claimed by Applicants.

A. **"Scheduled to enter an idle state":** Claims 1-5 and 10-24.

Claim 1 recites, in part, "***in response to a first processor in the plurality of processors being scheduled to enter an idle state*** ..." (Claim 1, in part, emphasis added). Claim 10 recites, in part: "***the first logical processor being scheduled to enter an idle state*** ...."

(Claim 10, in part, emphasis added). Claim 15 recites, in part: "***in response to the first logical processor being scheduled to enter an idle state***..." (Claim 15, in part, emphasis added). Claim 20 recites, in part: in response to a first processor in the plurality of processors being scheduled to enter an idle state ..." (Claim 20, in part, emphasis added).

The Office Action improperly parses these limitations too finely. This limitation is set off by commas, and is a phrase that should be considered as a whole. The Office Action claims that "scheduled" is disclosed at one portion of the Zalewski reference and that "idle state" is disclosed at another. Applicants object to such approach, and vigorously assert that Claims 1, 10, 15 and 20 are allowable because the Office Action has failed to make any prima facie showing of the limitations quoted in the preceding paragraph.

Applicants disclose at paragraph 06 that a logical processor may be idled by an operating system thread scheduler. Applicants disclose at Paragraph 07 that a thread scheduler 210 may decline to schedule a task for a logical processor and, if that happens, the processor executes an idling sequence. Thus, the processor may be scheduled to enter an idle state.

In contrast, Zalweski does not disclose nor teach a scheduler that does this. The cited portion of Zalewski set forth by the Office Action is puzzling. The Office Action states that "in response to a first processor in the plurality of processors being scheduled" is taught at Col 7, lines 61-63. First of all, as is stated above, this is an improper construction of the limitation. Second, the cited portion of Zalewski shows no such thing. The cited portion of Zalweski at Col 7, lines 61-63 merely indicates that a community may implement a user policy for hardware usage. There is absolutely no teaching here of a scheduler. The Office Action asserts that this section teaches that "user-defined situations are scheduled". This is just not so. ***Implementation***

of a user policy for hardware usage is not equivalent to scheduling a processor to enter an idle state.. The Office Action therefore fails to make a prima facie case of anticipation regarding Claims 1, 10, 15, and 20.

B. **"In response"**: Claims 1-5 and 10-24

The Office Action has failed to make a prima facie case of anticipation for Claims 1, 10 and 15 for another reason as well. Zalewsky does not disclose or teach the "in response" portion of the following limitations of Claims 1, 10 and 15. Claim 1: " in response to a first processor in the plurality of processors being scheduled to enter an idle state due to lack of scheduling tasks, making a processor execution resource previously reserved for the first processor available to any of the plurality of processors" (Claim 1 as amended, in part). Claim 10: "cause the first logical processor to make a processor execution resource previously reserved for the first processor available to a second processor in the plurality of processors in response to the first logical processor being scheduled to enter an idle state due to lack of scheduling tasks" (Claim 10 as amended, in part). Claim 15: "cause the first logical processor to make a processor execution resource previously reserved for the first processor available to a second processor in the plurality of processors in response to the first logical processor being scheduled to enter an idle state due to lack of scheduled tasks" (Claim 15 as amended, in part). Claim 20: "in response to a first processor in the plurality of processors being scheduled to enter an idle state due to lack of scheduled tasks, making a processor execution resource previously reserved for the first processor available to a second processor in the plurality of processors" (Claim 20 as amended, in part).

While each and every word of the claims is important, for purposes of the discussion in this paragraph it is simpler to consider the following pertinent language of the claims. Claim 1

recites "make a processor execution resource … available" "***in response*** to a first processor … being scheduled to enter an idle state due to lack of scheduling tasks." Similarly, Claim 10 recites "make a processor execution resource … available …***in response*** to the first logical processor being scheduled to enter an idle state due to lack of scheduling tasks …" Similarly, Claim 15 recites "make a processor execution resource … available … ***in response*** to the first logical processor being scheduled to enter an idle state due to lack of scheduled tasks …" Claim 20 recites "making a processor execution resource … available … in response to a first processor … being scheduled to enter an idle state due to lack of scheduled tasks …" Zalewsky does not teach or suggest these limitations.

Zaleswky teaches that a second operating instance brings a resource to an idle state only ***in response*** to a resource request from a first operating system instance (Zalewsky, Abstract) or a system administrator (Zalewski, Col. 4, lines 54-55). This is a result of the fact that Zalewsky is directed toward a scheme that allows one operating system instance to cooperate, via a push approach, to share a resource with another instance if requested to do so. The idle state is entered in Zalewsky as a result of a request from a "needy" instance or the system administrator.

The Office Action, in the rejection of Claim 10, asserts that Zalewsky teaches these elements at Col. 4, lines 62-65 and Col. 18, lines 36-38. The Office Action asserts that these passages show that "an idle state does exist in the system." (Office Action, page 5, rejection of claim 10). However, this is not enough to meet the burden that the Examiner faces. Applicants do not dispute that the Zalewsky system includes an idle state and discloses unowned and inactive states. The question is whether Zalewsky discloses entering the idle state "***in response***" to the limitations recited by Applicants. Zalewsky simply does not.

In contrast, Applicants have claimed a scheme that releases a resource ***in response*** to a logical processor becoming idle due to lack of work to be performed by that resource. Another logical processor may or may not need the resource at the time it is released. The idle state is entered if "no more tasks are scheduled for this logical processor" , (Application, paragraph 07), not in response to a request from another OS instance or system administrator. Thus, Applicants have claimed, and Zalewsky fails to teach, "***in response to*** a first processor in the plurality of processors being scheduled to enter an idle state due to lack of scheduled tasks, making a processor execution resource previously reserved for the first processor available ..." (Claim 1 as amended, in part, emphasis added). Similarly, Applicants have claimed, and Zalewsky fails to teach "cause the first logical processor to make a processor execution resource previously reserved for the first processor available to a second processor in the plurality of processors ***in response*** to the first logical processor being scheduled to enter an idle state due to lack of scheduling tasks." (Claim 10 as amended, in part, emphasis added). Similarly, Applicants have claimed, and Zalewsky fails to teach "cause the first logical processor to make a processor execution resource previously reserved for the first processor available to a second processor in the plurality of processors ***in response*** to the first logical processor being scheduled to enter an idle state due to lack of scheduled tasks" (Claim 15 as amended, in part, emphasis added). Similarly, Applicants have claimed, and Zalewsky fails to teach "***in response*** to a first processor in the plurality of processors being scheduled to enter an idle state due to lack of scheduled tasks, making a processor execution resource previously reserved for the first processor available to a second processor in the plurality of processors" (Claim 20 as amended, in part, emphasis added).

The rejection of Claims 1, 10, 15, and 20 must fail because the Office Action has failed to make a prima facie case of anticipation over Zalewsky, at least for one or more of the reasons set

forth above. In addition, Claims 2 – 9, which depend from Claim 1, are also allowable. In addition, Claims 11-14, which depend from Claim 10, are also allowable. In addition, Claims 16-19, which depend from Claim 15, are also allowable. In addition, Claims 21-28, which depend from Claim 20, are also allowable.

C. **"any of the plurality of processors"**: Claims 1-5

The Office Action has failed to make a prima facie case of anticipation for Claim 1 for another reason as well. As amended, Claim 1 recites: "making a processor execution resource previously reserved for the first processor available to any of the plurality of processors." Zalewsky does not teach, disclose or suggest this limitation. Indeed, Zalewsky expressly teaches away from this approach. Zalewsky's teaching is limited to directed exchange, where a resource is requested by a an instance (see request 1014 of Fig. 10A and description at Zalewsky, Col. 29, lines 55-67) and is migrated to that particular instance (see move of the resource 1028 of Fig. 10D and description at Zalewsky, Col. 30, lines 1-37). Thus, the Office Action has failed to make a prima facie case of anticipation because Zalewsky fails to teach or disclose "making a processor execution resource previously reserved for the first processor available to any of the plurality of processors." (Amended Claim 1, in part).

Applicants note that Zalewsky generally discloses that a quiesced resource may be placed into a pool of unassigned resources (Zalewsky, Col. 32, lines 25-30). However, Zalewsky discloses only that this may occur in response to direction of a system manager. That is, Zalewsky does not teach or disclose making a previously-reserved processor execution resource available to any of a plurality of processors "in response to a first processor in the plurality of processors being scheduled to enter an idle state due to lack of scheduling tasks." (Claim 1 as amended, in part). See discussion in Section B ("in response"), above.

The rejection of Claim 1 must fail because the Office Action has failed to make a prima facie case of anticipation over Zalewsky, at least for one or more of the reasons set forth above. In addition, Claims 2 – 9, which depend from Claim 1, are also allowable.

I. Claim Rejections -35 USC § 103(a)

The Office Action has rejected 6-9 and 25-28 under 35 U.S.C. 103(a) as unpatentable over Zalewski et al., US Patent No. 6260068 B1 (Zalewski). However, the Office Action has failed to meet its burden of makings it prima facie case of obviousness for the claims, and such rejections should be withdrawn.

The legal requirements for a prima facie case of obviousness are clear. "The examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness." MPEP § 2142. It is well established that *prima facie* obviousness is only established when the prior art reference (or references when combined) teach or suggest all the claim limitations. *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991) (MPEP 2144).

However, Applicant notes that the rejections of the claims under 35 USC 103(a) rely on the above discussed rejections of claims 1 and 20 as anticipated by Zalewski. Therefore because the rejections of claims 1 and 20 cannot stand, as argued previously, the rejections of claims 6-9 and 25-28 also cannot stand for at least this reason and should be withdrawn.

In addition, regarding Claim 6, the Office Action states that it would have been obvious to modify Zalewsky to include a wakeup signal. Claim 6 recites, in part: "The method of claim ~~5~~2 wherein the first processor being scheduled to execute a task further comprises the first processor receiving a wake up signal."

The reasoning of the Office Action is that it would have been obvious that a "wakeup signal is necessary to indicate to a processor that it is no longer idle." (Office Action, Page 8). However, this is just not so. In Zalewsky, there would be no reason to apply a wakeup signal because, as is discussed above, Zalewsky does not disclose putting a processor in an idle state "due to lack of scheduling tasks." (Claim 1, in part) (See discussion at Section I.B, above). In Zalewsky, there would be no reason to provide a wakeup signal to schedule new work because Zalewsky does not disclose idling a processor for lack of work in the first place.

Applicant reserves the right to argue other assertions made in rejecting these claims in the future.

Therefore as argued above, the rejections of all claims pending in the application, i.e. claims 1-28, should withdrawn and the claims allowed.

The Examiner is welcome to contact the Attorney of Record, Shireen Irani Bacon (Reg. No. 40,494) at 512.263.1250 to discuss any matters with the case. The Commissioner is hereby authorized to charge any fees in connection with this communication to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: September 19, 2007

/Shireen Irani Bacon/

Shireen Irani Bacon
Reg. No. 40,494

1279 Oakmead Parkway
Sunnyvale, California 94085-4040
(503) 439-8778